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IS 12970-2-2 (1992): Semiconductor devices - integrated circuits, Part 2: Digital integrated circuits - essential ratings and characteristics, Section 2: integrated circuits memories [LITD 5: Semiconductor and Other Electronic Components and Devices]

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IS 12970 (Part 2/Sec 2) : 1992
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अनुभाग 2 समाकलित परिपथ मेमोरी

Indian Standard

SEMICONDUCTOR DEVICES — INTEGRATED CIRCUITS

PART 2 DIGITAL INTEGRATED CIRCUITS — ESSENTIAL RATINGS AND CHARACTERISTICS

Section 2 Integrated Circuit Memories

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NEW DELHI 110002

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FOREWORD

This Indian Standard was adopted by the Bureau of Indian Standards, after the draft finalized by the Semiconductor Devices and Integrated Circuits Sectional Committee had been approved by the Electronics and Telecommunication Division Council.

This standard is one of the series of standards on integrated circuits and Section 2 of the series of standards on essential ratings and characteristics of digital integrated circuits, covering integrated circuit memories. This is to be read in cojunction with IS 12970 (Part 1) : 1990 and IS 12970 (Part 2/Sec 1) : 1992.

This standard is based on the IEC Pub 748-2 'Semiconductor devices integrated circuits: Part 2 Digital integrated circuits' issued by the International Electrotechnical Commission (IEC).

It is proposed to withdraw the IS 7441 (Part 1) : 1974, dealing with essential ratings and characteristics of digital integrated circuits, as soon as the clauses mentioned therein are covered in the new series [IS 12970 (Part 1/Sec 1 to 3)].

Indian Standard
SEMICONDUCTOR DEVICES — INTEGRATED CIRCUITS

PART 2 DIGITAL INTEGRATED CIRCUITS — ESSENTIAL RATINGS AND CHARACTERISTICS

Section 2 Integrated Circuit Memories

1 SCOPE

This standard covers the essential ratings and characteristics of digital integrated circuit memories.

2 REFERENCES

2.1 The following Indian Standards listed below are necessary adjuncts to this standard:

IS No.	*Title*
IS 1885 (Part 7/ Sec 5) : 1971	Electrotechnical vocabulary: Part 7 Semiconductor devices, Section 5 Integrated circuits and microelectronics
3715 (Part 1): 1971	Letter symbols for semiconductor devices: Part 1 General aspects (*first revision*)
12970 (Part 1) : 1990	Semiconductor devices — Integrated circuits: Part 1 General
12970 (Part 2/ Sec 1) : 1992	Semiconductor devices — Integrated Circuits: Part 2 Digital integrated circuits essential ratings and characteristics, Section 1 General

3 TERMINOLOGY

For the purpose of this standard (Part 2/Sec 2) the terms and definitions given in IS 1885 (Part 7/Sec 5) shall be applicable in addition to 3 of IS 12970 (Part 1) : 1990.

4 LETTER SYMBOLS

For the purpose of this standard, the letter symbols given in IS 3715 (Part 1) : 1971 shall be applicable.

5 STATIC AND DYNAMIC READ/WRITE MEMORIES AND READ-ONLY MEMORIES

5.1 Circuit Identification and Description

The provision of 5 of IS 12970 (Part 2/Sec 1) : 1992 shall apply.

5.2 Functional Specifications

5.2.1 *Block Diagram*

The provisions of **6.1** of IS 12970 (Part 2/Sec 1) : 1992 shall apply together with the following :

The block diagram should be sufficiently detailed to enable the individual functional units within the memory (for example, address decode, chip enable, 'buffer' output circuits, etc) to be identified, together with their external connections.

5.2.2 *Functional Description*

The functions performed by the circuit shall be specified and the following information shall be stated:

a) the total number of bits of information capable of being stored in the memory circuit;

b) the number of bits per word capable of being stored in the memory circuit;

c) the method of addressing;

d) the function(s) performed by each terminal, together with a statement of each control signal required, and the necessary sequence of instruction (*see also* **5.7.2.1**); and

e) for dynamic memories, the method of refreshing.

5.3 Ratings (Limiting Values)

5.3.1 Provision of **7** of IS 12970 (Part 2/Sec 1) : 1992 shall apply together with the following:

a) in **7.2.1** of IS 12970 (Part 2/Sec 1) : 1992 then the permissible excess values, their duration and the duty cycle should be stated;

b) two new characteristics to be added, as given below:

    1) power dissipation (where appropriate) maximum value of continuous power dissipation.

    2) input transition times (where appropriate), for dynamic memories minimum values.

5.4 Recommended Operating Conditions (Within the Specified Operating Temperature Range)

5.4.1 Provision of **8** of IS 12970 (Part 2/Sec 1) : 1992 shall apply together with:

If the device requires any pre-conditioning such as voltage sequencing, dummy cycles or signal sequencing before a valid operation, this pre-conditioning should be defined.

5.5 Static Electrical Characteristics for Bipolar Memories

5.5.1 Provision of **9** of IS 12970 (Part 2/Sec 1) : 1992 shall apply.

5.6 Static Electrical Characteristics for MOS Memories

5.6.1 Provision of **10** of IS 12970 (Part 2/Sec 1) : 1992 shall apply.

5.7 Dynamic Electrical Characteristics

Each electrical characteristic of **5.7.1** should be stated under specified electrical worst-case conditions with respect to the recommended range of supply voltage(s) as stated in **8.1** of IS 12970 (Part 2/Sec 1) : 1992.

Limit values as required by **5.7.1** or, if these are not mutually acceptable to manufacturer and user, typical values should be stated either:

a) over the specified range of operating temperatures (for example, as a curve), or

b) at a temperature of 25°C, and at the maximum and the minimum operating temperatures.

Alternative (b) should be used only if the worst-case value of the characteristic over the whole temperature range can be deduced from the values given at the specified temperatures.

In all cases, limit values applicable at 25°C should be stated.

5.7.1 *Times Characterising the Response of the Circuit*

The following times should be stated under specified conditions.

5.7.1.1 *Access times* (*see* Notes 1 and 2)

a) Read access time.

b) Access time from each enable and select signal specified for the memory (*see* Note 3).

c) Address access time (not applicable where the address information is not accepted until it is clocked into the memory).

Maximum values should be stated for each of these access times.

NOTES

1 Specified measurement conditions should be given in order to ensure that all control signals are applied early enough so that they do not affect the specified access times.

2 The reference conditions for the measurements of access times must include the maximum permissible values of set-up times.

3 Where a fixed sequence of enable and/or select signals is specified (*see* **5.7.2.1**) and the last of these signals always determines the actual access time, then only the access times for the first and last of the signals in this sequence need be stated.

5.7.1.2 *Sense recovery time (for read/write memories only)*

Maximum value.

NOTE — If both 'read' and 'write' functions are controlled by a single terminal, then 'read access time' and 'sense recovery time' will be the same, and only one of these times is required.

5.7.1.3 *Output disable times*

Output disable times from the end of each relevant enable and select signal.

Maximum values.

NOTE — The output disable time is the time interval between the cessation of a specified enable/select signal, and the instant at which the output data are no longer valid.

5.7.1.4 *Transition times* (*see* Note 1)

Transition times should be stated under specified conditions (*see* Note 2), depending on the following conditions:

a) if the typical value of transition time is comparable to (*see* Note 3), or greater than, the typical value of propagation time, then a maximum value of transition time should be stated;

b) if the typical value of transition time is less than 10 ns, a minimum value should be stated (*see* Note 4); and

c) if both conditions (a) and (b) are fulfilled, then both minimum and maximum values should be stated.

Transition times, when required should be stated for both directions of transition (that is t_{THL} and t_{TLH} should be stated).

NOTES

1 In general, values of these times that apply for each or both directions of transition of the output signal should be given. In some cases (for example, MOS memories), provided it is known that only one direction of transition is significant (for example, output voltage changing towards the supply voltage), only this value need be stated.

2 The specified conditions of measurement should include the characteristics of the input pulse and oscilloscope (or other appropriate measuring system) and the configuration and component values of the output loading network.

3 The transition time is considered comparable to propagation time if its value exceeds 50 percent of the value of propagation time.

4 The object here is to state when very short transition times may be obtained, which may give rise to overshoot and coupling problems using practical loads.

5.7.2 *Requirement at the Inputs to Ensure Correct Sequential Operation*

5.7.2.1 *Static memories*

The following timing requirements are applicable to static read/write memories and are in accordance with the general principles given in **11.3** of IS 12970 (Part 2/Sec 1).

A timing diagram should be given, comprising a complete set of signals that would be required to enable each functional operation of the memory to be set up and measured. This set up of signals should be in accordance with the control signals included in Item (d) of **5.2.2**.

The timing sequence to be used should be stated and all time intervals that need to be known by the user for correct operation of the memory should be stated.

In general, the following times should be stated.

a) Cycle times — Read cycle time, write cycle time and, where appropriate, read-write cycle time and/or write-read cycle time.

Minimum values.

NOTE — In (b) to (e) inclusive, the terms 'enable' and 'select' are being used synonymously, since no formal definitions have yet been agreed. Wherever the term 'enable/select' occurs, the term to be used is that which is appropriate to the memory being specified. It should be noted that the set-up and hold times given in (b) and (c) assume that the memory does not have a latch facility operated by the enable/select input. If it does, then set-up and hold times referenced to end-of-write and end-of-enable/select should be referenced to simply 'write or enable/select'.

b) Set-up times — Minimum values for the following :

   1) address set-up time before write, or address set-up time before enable/select (*see* Note 1);

   2) enable/select set-up time before end-of-write;

   3) data-in set-up time before end-of-write, for a stated minimum value of enable/select pulse duration (width) (*see* Note 1); or

   4) data-in set-up time before end-of enable/select, for a stated minimum value of enable/select pulse duration (width) (*see* Note 1); and

   5) for complex memories having more than one enable or select control signal, at least one additional set-up time for each additional enable or select signal is required.

NOTE — The choice of write or enable/select as the reference pulse depends on which one becomes inactive first, and this should be in accordance with the timing sequence given in **5.7.2.1**. If the relative sequence in which write and enable select become inactive is irrelevant, this should be stated and values for both (3) and (4) should be given.

For memory having no enable/select facility, values of (1) and (3) only are required (that is two times are required).

c) Hold times — By analogy with set-up times, minimum values for the following:

   1) address after end-of-write hold time or address hold time after end-of-enable/select (*see* Note 1);

   2) enable/select hold time after end-of-write or write hold time after end-of-enable/select (*see* Note 1);

   3) data-in hold time after end-of-write or data-in hold time after end-of-enable/select (*see* Note 1);

   4) for complex memories having more than one enable or select control signal, at least one additional hold time for each additional enable or select signal is required.

NOTE 1 — The choice of write or enable/select as the reference pulse depends on which one becomes inactive first, and this should be in accordance with the timing sequence given in **5.7.2.1**. If the relative sequence in which write and enable/select become inactive is irrelevant, this should be stated, and values for both options in i) and iii) should be given.

For a memory having no enable/select facility, values for (1) and (3) only are required (that is, two times are required).

d) Write recovery time — Minimum value.

NOTE — In some memories, write recovery time and address after end-of-write hold time are the same and only one of the quantities need be stated in such cases.

e) Pulse durations (widths) — Minimum values for the following:

   a) write pulse duration (width);

   b) where appropriate, enable/select pulse duration (width) [*see* item (4) of (b)].

5.7.2.2 *Dynamic memories*

The following timing requirements are applicable to dynamic read/write memories, and are in accordance with the general principles given in **11.2** of IS 12970 (Part 2/Sec 1) : 1992.

A timing diagram should be given, comprising a complete set of signals that would be required to enable each functional operation of the memory to be set up and measured. This set of signals should be in accordance with the control signals included in **5.2.2** (d).

The timing sequence to be used and all time intervals that need to be known by the user for correct operation of the memory should be stated. In general, the following times should be stated:

a) Memories with enable input, excluding memories with multiplexed address inputs.

   1) Set-up times

      i) Address set-up time before enable.

ii) Read set-up time before enable.

iii) Chip-select set-up time before enable, where appropriate.

iv) Write set-up time before enable.

v) Data-in set-up time before write.

vi) Data-in set-up time before enable.

Minimum values.

2) Hold times

i) Address hold time after enable.

ii) Read hold time after enable.

iii) Chip-select hold time after enable, where appropriate.

iv) Write hold time after enable, where appropriate.

v) Data-in hold time after enable.

vi) Data-in hold time after write.

Minimum values.

3) Cycle times

i) Read cycle time.

ii) Write cycle time.

iii) Read-modify-write cycle time, where appropriate.

iv) Read-write cycle time, where appropriate.

Minimum values.

4) Pulse duration (widths)

i) Read pulse duration (width).

ii) Write pulse duration (width).

iii) Enable pulse duration (width).

Minimum and, where appropriate, maximum values.

5) Precharge time

Minimum value.

6) Refresh time interval

Maximum value.

7) Transition times

i) Enable rise time.

ii) Enable fall time.

iii) Read-write mode select transition times, as appropriate.

Minimum and maximum values.

b) Memories with multiplexed address inputs

1) Set-up times

i) Row-address set-up time before row-address-select.

ii) Column-address set-up time before column-address select.

iii) Read set-up time before column-address-select.

iv) Data-in set-up time before column-address-select, where appropriate.

v) Data-in set-up time before write.

vi) Write set-up time before column-address-select.

vii) Write set-up time before row-address-select.

viii) Chip-select set-up time before column-address-select, where appropriate.

Minimum values.

2) Hold times

i) Column-address hold time after row-address-select.

ii) Read hold time after co'umn-address-select.

iii) Write hold time after column-address-select.

iv) Write hold time after row-address-select.

v) Data-in hold time after column-address-select.

vi) Data-in hold time after row-address-select.

vii) Data-in hold time after write.

viii) Chip-select hold time after row-address-select, where appropriate.

Minimum values.

3) Delay time between input signals

i) Delay time between column-address-select signal becoming inactive and row-address-select signal becoming active.

ii) Delay time between column-address-select signal becoming active and row-address-select signal becoming inactive.

Minimum values.

4) Cycle times

i) Read cycle time.

ii) Write cycle time.

- iii) Read-write cycle time, where appropriate.
- iv) Read-modify-write cycle time, where appropriate.
- v) Page cycle time, where appropriate.

Minimum values.

5) Pulse durations (widths)

- i) Row-address-select pulse duration (width).
- ii) Column-address-select pulse duration (width).
- iii) Write pulse duration (width).

Where appropriate, minimum and/or maximum values.

6) Precharge times

- i) Row-address-select precharge time.
- ii) Column-address-select to row-address-select precharge time.
- iii) Column-address-select precharge time.

Minimum, and where appropriate, maximum values.

7) Refresh time interval

Maximum value.

8) Transition times

- i) Row-address-select transition times.
- ii) Read/write transition times, as appropriate.
- iii) Enable (chip select) transition times.

Minimum and maximum values.

5.7.3 *Input and Output Capacitances*

Typical and maximum values of input and output capacitances under specified conditions.

5.8 Power or Current Drawn from Each Supply (Static Operation)

Maximum values of current into each supply terminal under worst-case conditions and for both active and standby modes if these are significantly different from each other. The typical values under nominal operating conditions should also be given.

5.9 Power or Current Drawn From Each Supply (Dynamic Operation)

Curve(s) showing the typical values of current required from the power supply(ies) *versus* the pulse repetition frequency, or typical values at two specified pulse repetition frequencies. This (these) should be given under specified recommended operating conditions.

Where appropriate, the above information should be given for clock inputs acting as pulsed power supplies.

Where appropriate, this information should also be given for standby operation.

5.10 Mechanical Ratings, Characteristics and Other Data

Any specific mechanical or environmental ratings applicable to the integrated circuit memory should be stated (*see* also **5.5** of IS 12970 (Part 1) : 1990.

5.11 Supplementary Information

5.11.1 *Output Loading Capability*

The maximum number of specified loads that can be driven from each output. This information may be given for more than one type of load.

5.11.2 *Noise Margins*

Information about the memory that enable noise margins to be calculated is given in **5.5** and **5.6** (*see also* **17.2** of Section 1 of IS 12970 (Part 2/Sec 1).

5.11.3 *Interconnections of Similar Units*

Examples of logic operations (for example, wired-OR) that may be performed by interconnecting similar memory units should be stated.

5.11.4 *Type of Output Circuit*

Information should be given regarding the type of output circuit, for example, three-state, open-collector, open-drain, push-pull.

5.11.5 *Interconnections to Other Types of Circuits*

Where, appropriate, details of the interconnections to other circuits, for example, sense amplifiers, buffers, should be given.

5.12 Handling Precautions

Provision of **8** of IS 12970 (Part 1) : 1990 shall apply.

6 FIELD-PROGRAMMABLE READ-ONLY MEMORIES

6.0 The material in this clause is intended to cover programmable and reprogrammable read-only memories, the latter being:

- a) either ultraviolet erasable and electrically programmable.
- b) or electrically erasable and electrically programmable.

6.1 Circuit Identification and Description

The provisions of **5** of IS 12970 (Part 2/Sec 1) shall apply, together with the following addition to **5.2** (Technology):

'This statement should also include details of the type of storage cell : diode matrix, fusible link, floating-gate avalanche-injection type, etc.'

6.2 Functional Specifications

6.2.1 *Block Diagram*

A block diagram or equivalent circuit information of the digital integrated circuit should be given.

The block diagram should identify the function of each external connection and, where no ambiguity may occur, can also show the terminal numbers. If the encapsulation has metallic parts, any connection to them from external terminals should be indicated. The connections with any associated external electrical elements should be stated, where necessary.

As additional information, the complete electrical diagram can be reproduced, but not necessarily with indications of the values of the circuit components.

The block diagram should be sufficiently detailed to enable the individual functional units within the memory (for example, address decode, chip enable, "buffer" output circuits, programming/erasing control circuits, etc) to be identified, together with their external connections.

6.2.2 *Identification of Terminals*

The following terminals should be identified on the block diagram:

a) supply terminals, that is, terminals intended to be connected to the power supplies;

b) input or output terminals, that is, terminals into which or out of which signals are passed. The term 'signal' include both pulse and more complex waveforms;

c) input/output terminals, that is, terminal that may function at different times as input or output terminals;

d) three-state output terminals, that is, output terminals that may be controlled to give a high-impedance condition;

e) multi-functional terminals, that is, terminals that may be used at different times for different functions, for example, programming and erasing.

6.2.3 *Functional Description*

The functions performed by the circuit should be specified and the following information should be stated:

a) the total number of bits of information capable of being stored in the memory circuit;

b) the number of bits per word capable of being stored in the memory circuit;

c) the method of addressing for read mode;

d) the function(s) performed by each terminal, together with a statement of each control signal required, and the necessary sequence of operations or instructions;

e) the method of programming;

f) the method of erasing the contents of the whole memory or a selected part of it;

g) output level in the unprogrammed state.

6.3 Ratings (Limiting Values)

The provisions of **7** of IS 12970 (Part 2/Sec 1) : 1992 shall apply, the following should be added:

a) in **7.2.1** : '......, then the permissible excess values, their duration and the duty cycle should be stated'.

b) new clause **7.5** : 'Maximum number of programming-erasing cycles permitted (where appropriate)'.

6.4 Read Mode

6.4.1 *Recommended Operating Conditions (With in the specified operating temperature Range)*

See **8** of IS 12970 (Part 2/Sec 1) : 1992.

6.4.2 *Static Electrical Characteristics*

The following electrical characteristics should be stated:

a) Input and output currents

   1) For bipolar integrated circuits, the requirements of **9** and **9.3** of IS 12970 (Part 2/Sec 1) : 1992, shall apply.

   2) For MOS integrated circuits, the requirements of **10**, **10.2.1** and **10.2.2** of IS 12970 (Part 2/Sec 1) : 1992, shall apply.

b) Input and output voltages

   1) For bipolar integrated circuits, the requirements of **9** and **9.1** of IS 12970 (Part 1/Sec 1) : 1992, shall apply.

   2) For MOS integrated circuits, the requiements of **10** and **10.1** of Section 1 of IS 12970 (Part 2/Sec 1), shall apply.

c) Input clamping voltage(s)

The requirements of **9.2** of IS 12970 (Part 2/Sec 1) : 1992 shall apply.

d) Output short-circuit current(s)

Maximum and/or minimum values.

e) Input and output leakage currents (where appropriate)

Maximum values.

f) Input and output capacitances

Typical and maximum values under specified conditions.

6.4.3 *Dynamic Electrical Characteristics*

6.4.3.1 *General*

The requirements of **5.7** concerning the conditions of supply voltages and operating temperatures applicable to dynamic electrical characteristics, apply.

6.4.3.2 *Times characterizing the response of the circuit*

The following electrical characteristics should be stated. They are intended to apply to the memory circuit after it has been programmed:

a) Access times

The requirements of **5.7.1.1** shall apply.

b) Output disable time(s)

The requirements of **5.7.1.3** shall apply.

c) Output data valid time(s)

Minimum value(s) from the end of each relevant enable and/or select signal.

d) Transition times

The requirements of **5.7.1.4** shall apply.

6.4.4 *Timing Requirements*

Where appropriate, any or all of the following timing requirements should be stated:

a) Set-up times

Minimum value(s)

(For example: 'Address' before 'Enable' set up time.)

b) Hold times

Minimum value(s)

(For example: 'Address' after 'Enable' hold time.)

c) Read cycle times

Minimum and/or maximum values.

6.5 Programming Mode

6.5.1 *Programming Procedure*

The recommended programming procedure should be stated. Where appropriate, the verification method and conditions (for example, sense voltage, static and dynamic characteristics of the programme pulses, number of programme pulses) during programming should be stated.

If an erasing procedure is necessary before programming, it should be specified.

6.5.2 *Recommended Programming Conditions*

The specified conditions for programming should be stated in accordance with **8** of IS 12970 (Part 2/ Sec 1).

When the temperature range to be used for the programming procedure is different from the operating temperature range, this should be specified.

The following electrical conditions and/or characteristics should be stated with maximum and/or minimum values:

a) power supply current(s) and/or voltage(s) when the programme pulse is applied;

b) programming current(s) and/or voltage(s) at specified terminals to which the programme pulse is applied; and

c) input current(s) and/or voltage(s) at any terminal for programming control.

6.5.3 *Timing Requirements*

6.5.3.1 *Devices having separate programme terminal(s)*

A timing diagram should be given, and the following timing requirements stated:

a) Programme pulse duration (width) .... minimum and maximum values

b) Programme pulse rise time .... minimum and/or maximum values

c) Programme pulse fall time .... minimum and/or maximum values

d) Programme duty cycle (where appropriate) .... maximum value

e) Set-up time ....

Minimum values should be stated for the following set-up times:

1) address before programme pulse or programme enable (*see* Note),

2) data-in before programme pulse or programme enable (*see* Note), and

3) programme enable before programme pulse (where appropriate).

f) Hold times ....

Minimum values should be stated for the following hold times:

1) address after end of programme pulse or programme enable (*see* Note);

2) data-in after end of programme pulse or programme enable (*see* Note);
3) address after end of data-in;
4) programme enable after end of programme pulse (where appropriate).

NOTE — The choice of 'programme pulse' or 'programme enable' as the reference pulse depends on which one becomes inactive first, and this should be in accordance with the given timing diagram.

6.5.3.2 *Devices without separate programme terminals*

Requirements are under consideration.

6.6 Erasing Mode (If Applicable)

The erasing procedure and the range of operating temperatures at which this operation may be carried out should be stated.

6.6.1 *Electrically Erasable Memories*

6.6.1.1 *Recommended erasing conditions*

The following electrical conditions during erasing should be stated, with maximum and/or minimum values:

a) power supply current(s) and/or voltage(s), when the erase pulse is applied;
b) erasing current(s) and/or voltage(s) at specified terminals to which the erase pulse is applied; and
c) input current(s) and/or voltage(s) at any other terminal used for an erasing operation.

NOTE — When the temperature range to be used for the erasing procedure is different from the operating temperature range, this should be specified.

6.6.1.2 *Timing requirements (erasure)*

a) Devices having separate erase terminals

The following timing requirement should be stated:

1) Erase pulse duration (width) .... minimum and maximum values
2) Erase pulse rise time .... maximum and/or minimum values
3) Erase pulse fall time .... maximum and/or minimum values
4) Erase duty cycle (where appropriate).......... maximum value.
5) Set-up times :
   i) address before start of erase pulse .... minimum value
   ii) enable before start of erase pulse (where appropriate) .... minimum value
6) Hold times
   i) address after end of erase pulse .... minimum value
   ii) enable after end of erase pulse (where appropriate) .... minimum value

b) Devices without separate erase terminals

Requirements are under consideration.

6.6.2 *Ultraviolet Erasable Memories*

6.6.2.1 *Recommended erasing conditions*

The following quantities, with their tolerances, should be stated:

a) ultraviolet light wavelength;
b) ultraviolet light intensity on the transparent window of the case; and
c) exposure time.

6.7 Number of Programming - Erasing Cycles

The minimum number of programming-erasing cycles that can be achieved for specified operating conditions should be stated.

NOTE — This number is likely to be a function of the programme and/or erase pulse conditions, the operating time and temperature.

6.8 Data Retention Information

Where appropriate, for example for electrically erasable and electrically programmable read-only memories, the following data retention information should be stated:

a) maximum number of read operations, and
b) minimum data retention time.

6.9 Power or Current Drawn from Each Supply (Static Operation)

Maximum values of current into each supply terminal at worst-case conditions and for both active and standby mode if these are significantly different from each other. Typical values at normal operating conditions should also be given.

6.10 Power or Current Drawn from Each Supply (Dynamic Operation)

Curve(s) showing typical values of current required from the power supply(ies) *versus* the pulse repetition frequencies or typical values at two specified pulse repetition frequencies. These should be given for specified recommended operating conditions for information purposes.

Where appropriate, the above information should be given for clocks acting as pulsed power supplies.

Where appropriate, this information should also be given for standby operation.

6.11 Mechanical Ratings, Characteristics and Other Data

Any specific mechanical or environmental ratings applicable to the programmable read-only memory should be stated (*see also* **5.5** of IS 12970 (Part 1) : 1990.

6.12 Supplementary Information

6.12.1 *Output Loading Capability*

The maximum number of specified loads that can be driven from each output. This information may be given for more than one type of load.

6.12.2 *Electrical Noise Margins*

Information about the programmable read-only memory that enables noise margins to be calculated is given in **17.2** of IS 12970(Part 2/Sec 1) : 1992.

6.12.3 *Interconnections of Similar Units*

Examples of logic operations (for example wired-OR) that may be performed by interconnecting similar memory units should be stated.

6.12.4 *Type of Output Circuit*

Information should be given regarding the type of output circuit, for example, three-state, open-collector, open-drain, push-pull (totem-pole).

6.12.5 *Interconnections to Other Types of Circuits*

Where appropriate, details of the interconnections to other circuits, for example, sense amplifiers, buffers, should be given.

6.13 Handling Precautions

Where appropriate, the following information should be stated:

a) handling precautions, as in **8** of IS 12970 (Part 1) : 1990 for electrostatic sensitive programmable read-only memories;

b) precautions necessary to avoid excessively high voltages during programming;

c) special conditions after programming, for example, covering the transparent window to prevent the exposure to detrimental light in the case of ultraviolet erasable read-only memories;

d) precautions to be observed against electromagnetic and nuclear radiation.

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